B1 cont.

used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used.

B2

10. (Amended) The semiconductor memory device of claim 8, wherein the control unit controls ON/OFF of the source voltage supplied to the entire DRAM memory block in response to a control signal which is externally supplied to the control unit.

B3

13. (Amended) A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including an SRAM cell array;

a DRAM memory block provided on the chip, the DRAM memory block having a DRAM cell array; and

a control unit connected to each of the SRAM memory block and the DRAM memory block, the control unit including a first pad and a second pad, the control unit activating an operation of one of the SRAM memory block or the DRAM memory block based on a combination of a first control value indicated by a first control signal presented to the first pad and a second control value indicated by a second control signal presented to the second pad,

wherein the control unit activates or deactivates operation of the DRAM memory block via the first and second pads, depending on whether the DRAM cell array is used to retain data, so that the operation of the DRAM memory block is deactivated when the DRAM cell array is not used.

REMARKS

The Office Action dated February 2, 2003 has been received and carefully noted. The following remarks are submitted as a full and complete response. Claim 9 is canceled. Claims 8, 10 and 13 are amended. No new matter is added. In view of the above amendments and the following remarks, favorable consideration of claims 8, 10, 13 and 14 is respectfully requested.

The Office Action rejected claims 8-10 and 13-14 under 35 U.S.C. §103(a) as being